A Hybrid Filter for the Suppression of Common-Mode Voltage and Differential-Mode Harmonics in Three-Phase Inverters With CPPM

Jin Huang, *Member, IEEE*, and Haixia Shi

***Abstract*—In the motor systems driven by sinusoidal pulse width modulation (SPWM) three-phase inverters, the peaks of common-mode (CM) voltage are so high that it will cause many negative effects. In this paper, a hybrid filter is presented to reduce the CM voltage (CMV) and the differential-mode (DM) harmonics in a three-phase inverter with carrier peak position modulation (CPPM). Because the use of CPPM strategy in the inverter can ensure that the output CMV will be only two levels in any condition, the simple active CM filter (composed of a half-bridge circuit) in the hybrid filter can effectively suppress the output CMV and CM current. The passive filter in the hybrid filter consists of an added single tuned filter and the original DM low-pass filter. The single tuned filter is designed to lower the DM harmonics, which are aggravated by the CPPM strategy in the carrier frequency band. Through the experiments, the validity of CMV and DM harmonics suppression by the hybrid filter in the three-phase inverter is verified and the calculation-control active CM filter is proved to be the best in the optional schemes.**

***Index Terms*—Carrier peak position modulation (CPPM), common-mode voltage (CMV), differential-mode (DM) harmonics, hybrid filter, sinusoidal pulse width modulation (SPWM).**

I. Introduction

SWITCHED-MODE power supplies are more and more widely used in industrial equipments. But this switched mode will bring many negative effects. In the motor regulation systems driven by pulse width modulation (PWM) inverters, the peaks of output common-mode (CM) voltage are very high due to the instantaneous imbalance of three phase voltages. The CM voltage (CMV) will produce a huge pulsating CM current (CMC) through the distributed capacitance of the system. The CMC could interfere with the adjacent devices along the ground wire and even will result in the wrong operation of the devices [1], [2]. In addition, the CMV will cause the high shaft voltage through the parasitic capacitors between the stator and the rotor. The high shaft voltage could lead to momentary electromagnetic discharge phenomena (viz. the bearing current) [3]–[5] and will therefore damage the motor bearing [6], [7].

In recent studies, some optimized control strategies are used to reduce the output CMV in the three-phase inverter. For the inverter with the space vector modulation (SVM) strategy, the CMV is reduced by using nonzero vectors to synthesize zero vectors [8]–[10]. For the inverter with the discontinuous PWM (DPWM) strategy, the CMV is reduced by avoiding the generation of zero vectors. In this method, three triangular carriers with various polarities are used to modulate three reference voltages. Under different carrier polarity combinations there are different DPWM methods [11], [12], such as active zero state PWM (AZSPWM) [13], remote state PWM (RSPWM) [14], [15], near state PWM (NSPWM) [16], and so on.

For the sinusoidal PWM (SPWM) control inverter, the CMV can be reduced by using the carrier phase shift (CPS) strategy [17]. But in the application of the CPS strategy, the modulation index M_a of SPWM must be limited to $M_a < 2/3$. In order to break through the limitation of the modulation index, the strategy of carrier peak position modulation (CPPM) is adopted [18].When the zero state appears, instead of the usual symmetric triangular carrier, an oblique triangular carrier is used to modulate the reference voltage. Thus, the zero state is avoided and the CMV is reduced.

In the inverter system, the peak value of the output CMC is influenced by the CMV dv/dt and the distributed capacitance of the system. When the system is established, the CMV dv/dt plays a decisive role in the CMC. In aforementioned strategies, although all the output CMVs of inverters can be reduced to $\pm V_{\rm dc}/6$ ($V_{\rm dc}$ is the dc-side voltage of inverters), the step level of CMV is still $V_{\rm dc}/3$ when their switches are switching. So the peak of CMC will not be reduced. Only with the aid of a CM filter could more CMV and CMC be reduced. CM filters can be divided into passive and active ones.

Most passive filters are realized with two common ways: a CM choke [19]–[21] or CM transformer [22]–[24] cascading into the main circuit; a resistor-capacitor (RC) or resistor-inductor-capacitor (RLC) attenuation network paralleling into the main circuit [25]–[27]. The drawbacks of passive CM filters are as follows: its bulky size, high power loss, etc.

Active CM filters are of more popular concern. In some active filters, the active devices are working in the linear

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J. Huang is with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: huangjin.mail@163.com).

H. Shi is with Wuhan Textile University, Wuhan 430073, China (e-mail: shi.haixia@163.com).

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region and the reversal voltage is produced to compensate the CMV of the three-phase inverter [28]–[30]. Although the suppression effect of CMV is excellent under this method, it is difficult to implement this type of filters in high-voltage cases because of the linear area restriction for analog push-pull transistors.

The active power filter composed of switching circuits is not affected by the limit of voltage class. In the conventional SPWM or SVM three-phase inverter, the CMV is a four-level pulse. So the active filter is implemented by using a multi-level inverter and the four-level voltage is yielded to counteract the CMV [31]. The structure of this multi-level active filter is too complex to be used in the low cost cases. In the above active filters, all the compensative voltages are cascaded into the inverter's output through a CM transformer. The CM transformer is complex in design and manufacture, big in size, and not easy to be installed because of the cascade mode, which is especially not propitious for the revamping of the established inverter. In the inverter with CPS, the CMV is suppressed by using three-phase four-leg topology [17]. Because the modulation index under the CPS strategy is limited, the application of this filter is restricted.

This paper describes the design of a hybrid filter in the three-phase inverter with CPPM. Under the CPPM strategy, the output CMV of the inverter will be only two levels in all cases. So the active CM filter in the hybrid filter is designed to be a simple half-bridge structure, which can be used to counteract almost all the CMV. The counteract voltage is paralleled into the inverter's output, which is convenient for the installation of the filter. When the carrier frequency f_c is relatively low in the three-phase inverter with CPPM, the differential-mode (DM) harmonics in the carrier frequency band will be substandard. To solve this problem, a single tuned filter is added in the hybrid filter. The single tuned filter and the existing low-pass filter form a passive DM filter. Thus the hybrid filter is designed not only to suppress the CMV but also to make the DM voltage (DMV) comply with standards. In Section II, the CMV in the three-phase inverter is reviewed briefly. Section III presents the fact that the phase-shifting of the carrier affects the output DMV of the inverter in theory and shows the simulation results accordingly. In Part A of Section IV, the designing process of the active CM filter is expounded. The single tuned filter is shown in Part B of Section IV. The implementation of the hybrid filter is discussed in Part C of Section IV. The experimental results of the three-phase inverter with or without the hybrid under different strategies are compared in Section V. Finally, the conclusions are drawn in Section VI.

II. CMV in Three-Phase Inverter

In the three-phase inverter as shown in Fig. 1, the output CMV v_{cm} can be expressed as

$$v_{\rm cm} = (v_a + v_b + v_c)/3 \tag{1}$$

where v_a, v_b, and v_c are the output voltages of three legs respectively.

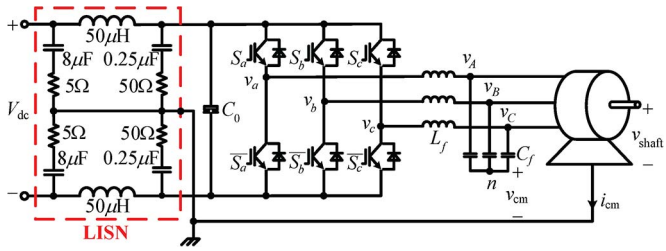

Fig. 1. Three-phase inverter.

Fig. 2(a) shows the CMV in the three-phase inverter with the conventional SPWM strategy. When v_a, v_b, and v_c are of high (or low) level, which is called the zero state, the peaks of the output CMV are maximal (about $\pm V_{\rm dc}/2$). The zero state is the major cause of the huge CMV. If the peaks of three carriers are mutually staggered $T_c/3$ (T_c is the carrier cycle) in the inverter, the probability for the occurrence of the zero state will be the lowest. This is the key idea of the CPS strategy [17]. As shown in Fig. 2(b), the occurrence frequency and the duration time of $\pm V_{\rm dc}/2$ in CMV are reduced greatly.

In order to avoid the zero state in all cases, the variant oblique triangular carrier is used to modulate the reference sinusoidal voltage instead of the usual symmetric triangular carrier in the inverter with the CPPM strategy. Fig. 2(c) shows that the peaks of the output CMV with CPPM are reduced to $\pm V_{\rm dc}/6$. The problem of the switching dead-time has been considered in the calculation of carrier peak positions [18]. Thus, using the CPPM strategy can ensure that the output CMV of the inverter will appear only two-level voltage $(\pm V_{\rm cd}/6)$ in any case.

III. Harmonics of DMV

For the asymmetrical regular-sampled SPWM, the output voltage of Phase r $(r = a, b, c)$ in the three-phase inverter can be expressed by (2) [32]. In (2), $J_n[\bullet]$ is the nth order Bessel function; f_0 is the output power-frequency; m is the carrier index; n is the baseband index; $q = m + nf_0/f_c$; θ_{rc} and θ_{r0} are the initial phases of the carrier and the reference sinusoid respectively. θ_{rc} and θ_{r0} of the inverter under the conventional SPWM strategy or under the CPS strategy are listed in Table I.

In view of (2) and the initial phase data (see Table I), the DMV v_{ab} between Leg A and Leg B of the three-phase inverter under the conventional SPWM strategy can be deduced. Its result is revealed in (3). In the similar manner, the DMV under the CPS strategy can be got by (4).

$$v_r(t) = \frac{2V_{\rm dc}}{\pi} \sum_{\substack{m=0\leftrightarrow \\ m>0\leftrightarrow}}^{\infty} \sum_{\substack{n=1 \\ n=-\infty}}^{\infty} \frac{1}{q} J_n\left(\frac{qM_a\pi}{2}\right) \sin\left[\frac{(m+n)\pi}{2}\right] \cos\left[m(2\pi f_c t + \theta_{rc}) + n(2\pi f_0 t + \theta_{r0})\right] \tag{2}$$

$$v_{ab,\rm SPWM}(t) = -\frac{4V_{\rm dc}}{\pi} \sum_{\substack{m=0\leftrightarrow \\ m>0\leftrightarrow}}^{\infty} \sum_{\substack{n=1 \\ n=-\infty}}^{\infty} \frac{1}{q} J_n\left(\frac{qM_a\pi}{2}\right) \sin\left[(m+n)\frac{\pi}{2}\right] \sin\left(n\frac{\pi}{3}\right) \sin\left[2\pi(mf_c + nf_0)t - n\pi/3\right] \tag{3}$$

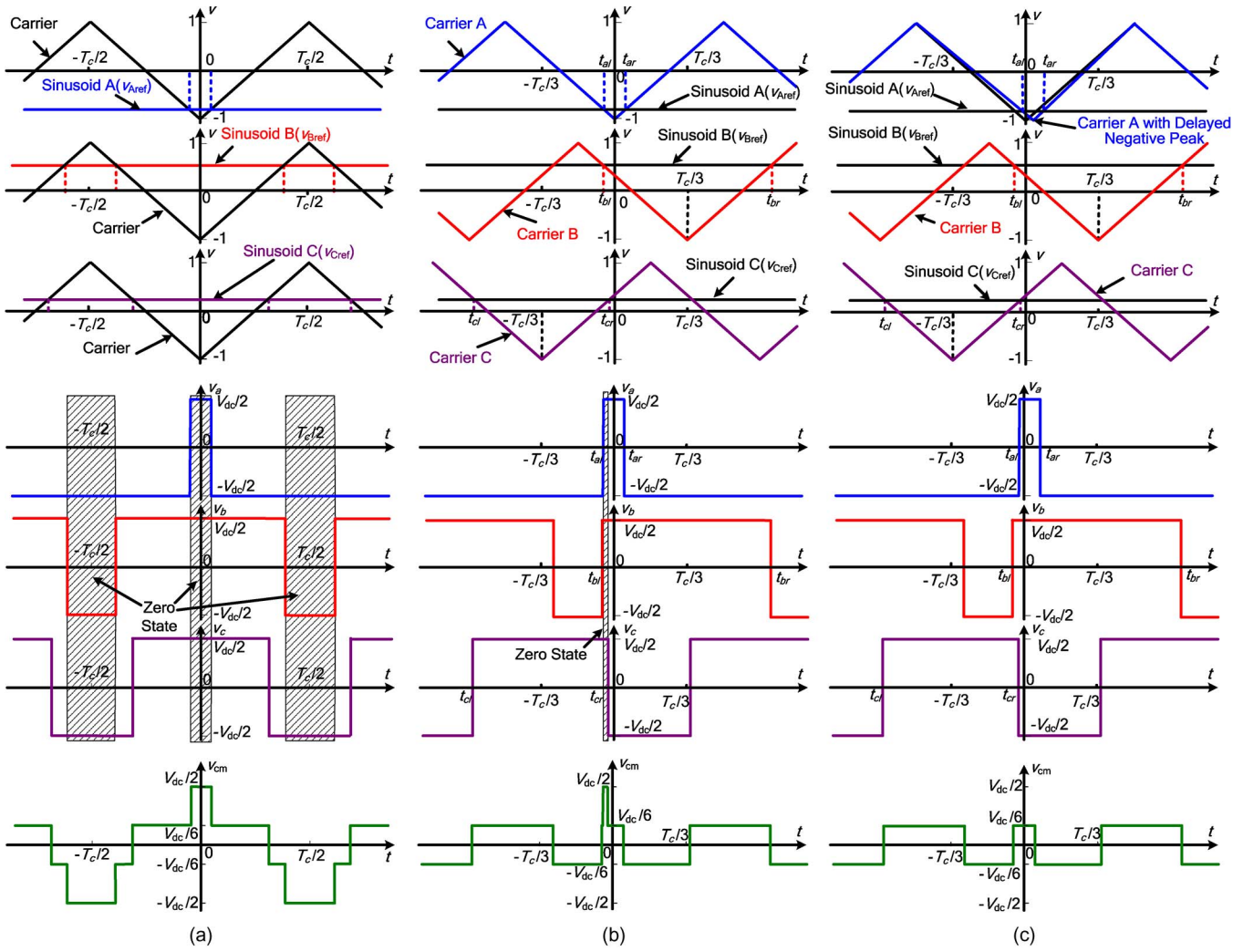

Fig. 2. Modulation of three-phase reference voltages with different carriers (top), three-phase output pulses (middle) and output CMVs (bottom) in the three-phase inverter under (a) the conventional SPWM strategy, (b) the CPS strategy, and (c) the CPPM strategy.

TABLE I
INITIAL PHASES OF DIFFERENT LEGS

Strategy	Leg A		Leg B		Leg C	
	θ_{ac}	θ_{a0}	θ_{bc}	θ_{b0}	θ_{cc}	θ_{c0}
Conventional SPWM	0	0	0	-2π/3	0	2π/3
CPS	0	0	-2π/3	-2π/3	2π/3	2π/3

$$v_{ab,\mathrm{CPS}}(t) = -\frac{4V_{\mathrm{dc}}}{\pi}\sum_{\substack{m=0\leftrightarrow\\ m>0\leftrightarrow}}^{\infty}\sum_{\substack{n=1\\ n=-\infty}}^{\infty}\frac{1}{q}J_n\left(\frac{qM_a\pi}{\pi 2}\right)\sin\left[(m+n)\pi/2\right]\sin\left[(m+n)\pi/3\right]\sin\left[2\pi(mf_c+nf_0)t-(m+n)\pi/3\right]. \quad (4)$$

Under different strategies, the DMVs of the three-phase inverter with no-load (i.e. load impedance is infinite) are simulated. The simulated parameters are listed in Table II. The switching dead-time is not considered in the simulations. The output DMV behind L_fC_f filter in the three-phase inverter

$$v_{AB}(f) = v_{ab}(f)/(1-4\pi^2L_fC_ff^2). \quad (5)$$

TABLE II
SIMULATED PARAMETERS IN THREE-PHASE INVERTER

Symbol	Value	Commentary
V_{dc}	700 V	DC-side voltage
L_f	900 μH	Inductor of low-pass filter
C_f	25 μF	Capacitor of low-pass filter
f_0	50 Hz	Output power-frequency

Fig. 3 shows the simulated fast Fourier transform (FFT) results of the DMV v_{AB} under three strategies at $f_c = 3.6$ kHz. The maximal harmonic peak of DMV usually appears at the carrier frequency. In the inverter with the conventional SPWM strategy, the $\sin(n\pi/3)$ [emphasized by dots in (3)] will cause the magnitude of DMV at f_c (viz. $m = 1, n = 0$) to be zero, and the $\sin[(m+n)\pi/2]$ [emphasized by small triangles in (3)] will cause the magnitudes of DMV at the adjacent frequencies of f_c (viz. $m = 1$, $n = \pm 1$) to be zero. In this case, the harmonic peak of DMV will appear at the frequency of $f_c - 2f_0$ or $f_c + 2f_0$ [at 3.5 kHz or 3.7 kHz as shown in Fig. 3(a)].

According to (4), the magnitude of DMV under the CPS strategy at f_c will not be zero and even will be large. Although the harmonics of the output DMV will be somewhat reduced

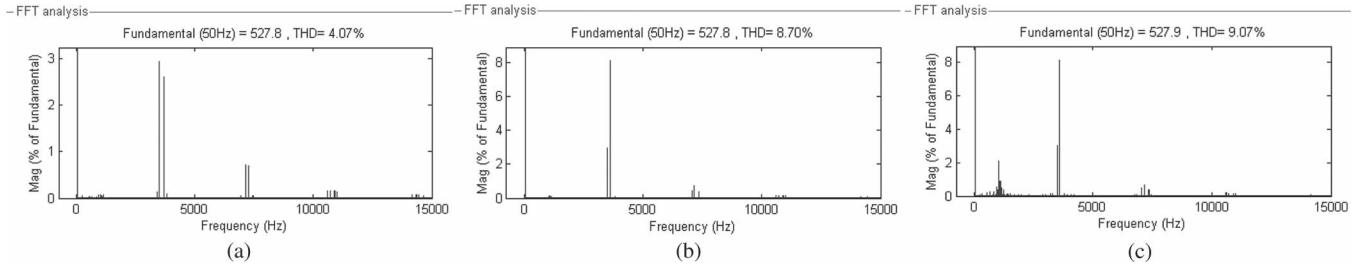

Fig. 3. Simulated FFT results of output DMV in the inverter under the (a) conventional SPWM strategy, (b) CPS strategy, and (c) CPPM strategy at $f_c = 3.6$ kHz.

TABLE III
SIMULATED THD OF OUTPUT DMV

Carrier frequency (kHz)	THD		
	Conventional SPWM	CPS	CPPM
2.5	9.42%	20.17%	20.34%
3.6	4.07%	8.70%	9.07%
5.0	2.03%	4.31%	4.56%
10.0	0.56%	1.11%	1.20%

through the low-pass filter (see L_fC_f in Fig. 1), the total harmonic distortion (THD) of DMV would be serious and even be substandard when the designed carrier frequency is low. In Fig. 3(b), the magnitude of the DMV harmonic at f_c is still about 8% of the fundamental magnitude despite the fact that the low-pass filter is used. The harmonic at f_c accounts for most of the harmonic components in the THD and causes the THD to go beyond the limit (viz. 3%–5%) that is usually demanded by the load [33].

The CPPM strategy is based on the CPS strategy. The difference between them is that the carrier peak position is changed for a short time in a small range [18]. Hence the output DMV harmonics in the inverter with CPPM will be similar to that with CPS. Compared Fig. 3(c) with Fig. 3(b), we can see that the harmonic magnitude in the carrier frequency band is almost the same and the THD in Fig. 3(c) is slightly higher.

Table III lists the simulated DMV THDs under different carrier frequencies. Under the condition of low f_c, if the CMV is suppressed by using the CPPM strategy, an extra DM filter is needed to reduce the harmonics in the carrier frequency band.

IV. HYBRID FILTER

In this paper, the primary task of the designed filter is to suppress the output CMV in the three-phase inverter. Using the CPPM strategy can ensure that the output CMV will be only two-level voltage in any case (see Section II). Thus, to suppress the CMV, a simple switching circuit can be designed as an active CM filter to produce the two-level voltage, which is the reversal of the original CMV. Meanwhile, a special design of DM filter aims at the suppression of the DMV harmonics in the carrier frequency band, because the DMV harmonics will make the THD exceed the standards (see Section III). The organic combination of the active CMV filters and the passive DMV filter forms the hybrid filter in this paper.

A. Active CM Filter

In the design procedure of the active CM filter, the switching circuit structure must be determined in accordance with the characteristic of the CPPM strategy firstly. Secondly, the coupling mode of the filter output must be designed. Lastly, the acquisition mode of the CMV signal must be selected.

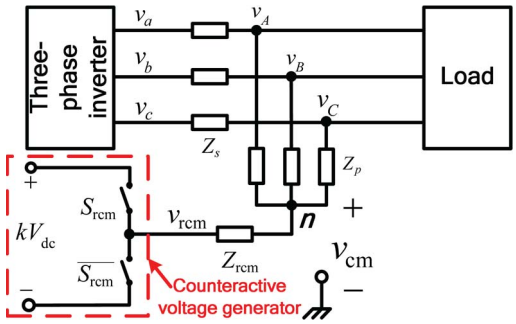

Fig. 4. Structure of the active CM filter.

Because the output CMV in the inverter with CPPM is a two-level voltage, a single-phase inverter structure can be designed to generate a reverse two-level voltage to the CMV. There are full-bridge structure and half-bridge structure in single inverters. In view of the cost, the simple half-bridge structure is the best choice. As shown in Fig. 4, the output voltage $v_{\rm rcm}$ of the half-bridge is $\pm kV_{\rm dc}/2$. The counteractive voltage of the CMV can be generated. The class of the dc-side voltage in the active CM filter can be changed by the proportional coefficient k. This is useful for the flexibility in choosing switching devices.

There are two ways by which the active CM filter is coupled into the main circuit of the three-phase inverter. In the first way, the three-phase CM transformer with wideband is cascaded in the main circuit of inverter and the compensation of the CMV is in the form of voltage. Because of the drawbacks that are pointed out in Section I, this way is not considered in this design.

In the second way of compensating the CMV, the output current of the active circuit is injected into the main circuit through the filter network in parallel (as shown in Fig. 4). The essence of this method is to change the potential of the neutral point n and to make it close to zero in theory.

According to Fig. 4, the CMV of the inverter's output is

$$v_{\rm cm} = \frac{(v_a + v_b + v_c)Z_{\rm rcm} + v_{\rm rcm}(Z_s + Z_p)}{(Z_s + Z_p) + 3Z_{\rm rcm}} \tag{6}$$

where $Z_{\rm rcm}$ is the output equivalent impedance of the active circuits in the filter network, and Z_s and Z_p are, respectively, the series impedance and the parallel impedance of the inverter's output. According to (6), if $v_{\rm rcm}$ is controlled as follows:

$$v_{\rm rcm} = -Z_{\rm rcm}(v_a + v_b + v_c)/(Z_s + Z_p). \tag{7}$$

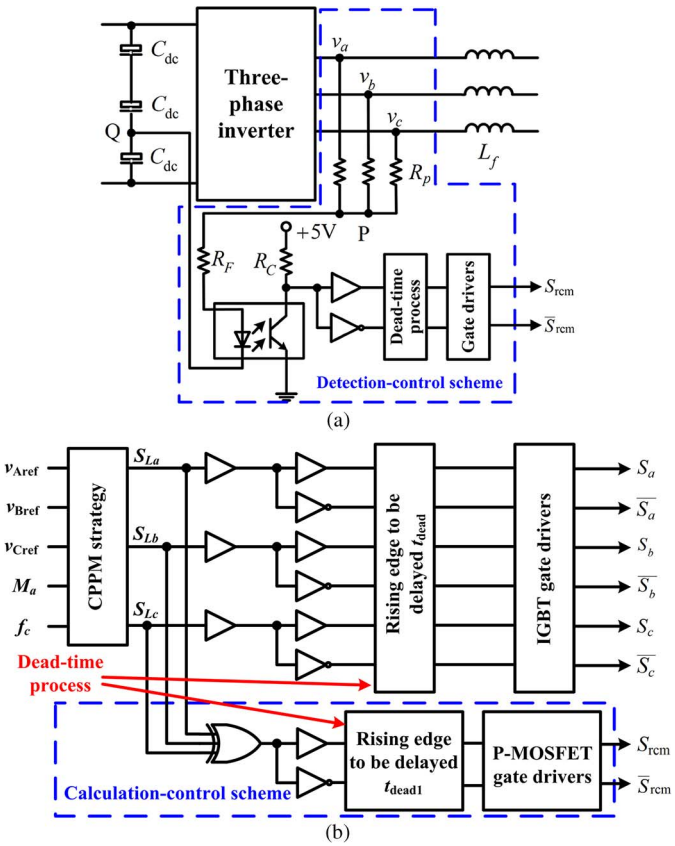

Fig. 5. Generation for the control signals of the active CM filter under (a) the detection-control scheme, and (b) the calculation-control scheme.

$v_{\rm cm}$ will be zero in theory. Because $v_{\rm rcm} = \pm kV_{\rm dc}/2$, $v_a + v_b + v_c = \pm V_{\rm dc}/2$, and they are opposite to each other, the design results can be obtained as follows

$$v_{\rm rcm} = -k(v_a + v_b + v_c) \tag{8}$$
$$Z_{\rm rcm} = k(Z_s + Z_p). \tag{9}$$

According to (8), the control signal $S_{\rm rcm}$ of an active filter's switch should have the reverse polarity to the signal $v_a + v_b + v_c$. Two schemes can be used to obtain the control signal $S_{\rm rcm}$. The first is the "detection-control" scheme. It means that $S_{\rm rcm}$ is obtained from measuring the polarity of the voltage $v_a + v_b + v_c$ directly and reversing it. As shown in Fig. 5(a), the signal is from a Y-type CMV detection circuit, which is made up of three R_p resistors. It is connected to the logic circuit, the dead-time process circuit, and the gate driver through an optocoupler. One terminal of the optocoupler is Point P (its potential is $\pm V_{\rm dc}/6$ under the CPPM strategy), the other is Point Q (its potential is $-V_{\rm dc}/6$). Such connection can ensure that the optocoupler input and the CMV have the same polarity.

This scheme can avoid the problem that the switching dead-time of three-phase inverters would have the negative impact on the control signal $S_{\rm rcm}$. However, this scheme has two weak points. One is the delay from "detection" to "control." The other is that the active counteractive circuit has its own switching dead-time problem. To solve the former problem, a faster optocoupler can be adopted to detect the voltage and the signal process should be simplified as far as possible in the implementation. Thus the delay time of detection-control will be shortened. To solve the latter problem, the devices with short switching dead-time can be adopted. Considering the need of short switching dead-time devices and the fact that the switch frequency of the active counteractive circuit is the triple of the carrier frequency in the three-phase inverter, it will be a good plan to select power metallic oxide semiconductor field effect transistors (P-MOSFETs) and anti-parallel fast recovery diodes as the switches in the active circuit.

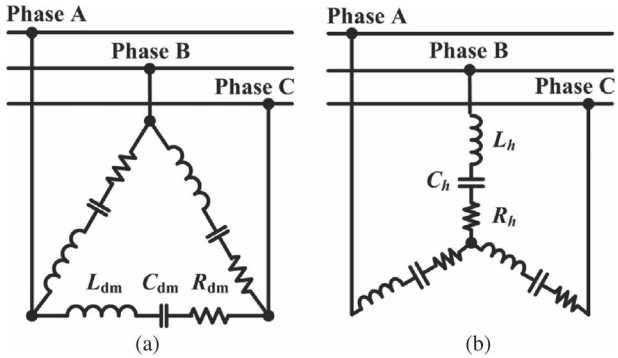

Fig. 6. Three-phase single tuned filter. (a) Δ-type and (b) Y-type.

The second way to obtain $S_{\rm rcm}$ is the "calculation-control" scheme. Under this scheme, the signal $S_{\rm rcm}$ is calculated in the processor as the following:

$$S_{\rm rcm} = S_{La} \oplus S_{Lb} \oplus S_{Lc} \tag{10}$$

where S_{La}, S_{Lb} and S_{Lc} are the control logic signals of the top switches of Leg A, Leg B, and Leg C, respectively [see Fig. 5(b)]. The delay of the detection-control process is avoided and no extra detection circuit is needed by using this scheme. But as a result of the switching dead-time control, it will not be ensured that the direction of a leg's actual output voltage (e.g. v_a) and its control logic signal (e.g. S_{La}) would be the same all the time. Such output voltage $v_{\rm rcm}$ with $S_{\rm rcm}$ [by (10)] can not be guaranteed to be the reverse of $v_a + v_b + v_c$ every moment either.

Because the actual influence of the switching dead-time on the leg's voltage is related to the equivalent impedance of the load, it is very difficult to be predicted in theory. Therefore, the above two schemes need to be compared and carefully chosen through experiments.

B. Passive DM Filter

Under the conventional SPWM control, the THD of the output DMV in the three-phase inverter will be guaranteed to be less than the regulation limit through the design of L_fC_f filter. As analyzed in Section III, the THD of the output DMV in the three-phase inverter with CPPM is substandard markedly when the carrier frequency is low. Since most harmonic energy locates in the carrier frequency band [see Fig. 3(c)], filtering out the harmonics near the carrier frequency can greatly improve the DM characteristic of the inverter's output.

What needs to be suppressed is mainly the carrier frequency harmonics, so a simple single tuned filter can be adopted to parallel in the line–line output of the three-phase inverter. There are two types of three-phase single tuned filters (see Fig. 6). In

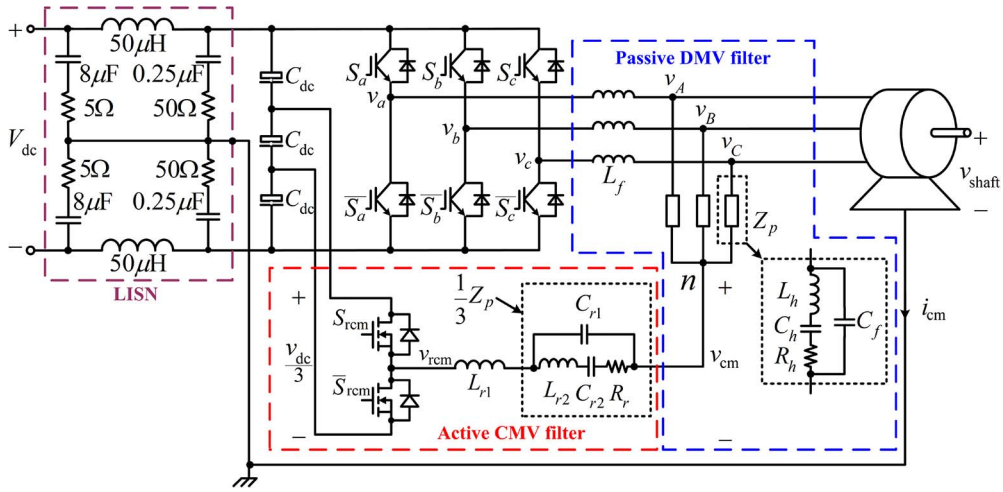

Fig. 7. Three-phase inverter with the hybrid filter.

view of the connection with the active CM filter, the Y-type filter is better than the Δ-type one. If the inductor L_h and the capacitor C_h in Fig. 6(b) are designed to satisfy

$$f_c = 1/\left(2\pi\sqrt{L_h C_h}\right) \tag{11}$$

the single tuned filter can greatly suppress the harmonics near the carrier frequency.

Because a capacitor C_f in the original low-pass filter is in parallel with a branch circuit of the single tuned filter, they can be merged into the impedance Z_p (as shown in Fig. 7). The passive DM filter is composed of the inductors L_f in the original low-pass filter and the impedances Z_p.

In theory, the THD of the output DMV can also be reduced by simply increasing the C_f of the original low-pass filter. But the previous studies [34], [35] show that a single tuned filter with a parallel capacitor has higher cost performance than a single capacitor in the harmonic suppression.

C. Hybrid Filter

It will form an organic whole to connect the above designed active CM filter with the passive DM filter through the neutral point n. That is the hybrid filter in the design plan (see Fig. 7).

In Fig. 7, the proportional coefficient k, which is mentioned in Part A of Section IV, is set 1/3. From Fig. 7, it can be seen that the mid-point of the inverter dc input is equipotential with the ground in essence because of the Line Impedance Stabilization Network (LISN). Then the voltage at any point is equal to the potential difference from the point to the mid-point of the dc input. Because the output CMVs of the inverter with the CPPM strategy are $\pm V_{\rm dc}/6$, the dc input voltage levels of the active CM filter must also be $\pm V_{\rm dc}/6$ when $k = 1/3$. So the dc voltage of the active filter can be taken from the divided voltage of the inverter dc voltage through the middle capacitor which is one of the series capacitors on the inverter dc-side. The potentials of the middle capacitor's two ends are just $\pm V_{\rm dc}/6$.

In accordance with the existing experience and rules [33], [36], the element parameters (L_f, C_f, L_h, C_h, and R_h) in the passive DM filter can be deduced. From (9), the element parameters of the active filter's output should be obtained by $L_{r1} = L_f/3$, $C_{r1} = 3C_f$, $L_{r2} = L_h/3$, $C_{r2} = 3C_h$, and $R_r = R_h/3$. The detailed parameters are listed in Table IV.

TABLE IV
EXPERIMENTAL PARAMETERS IN THREE-PHASE INVERTER

Symbol	Value	Commentary
$V_{\rm dc}$	700 V	DC-side voltage
L_f	900 μH	Inductor of low-pass filter
C_f	25 μF	Capacitor of low-pass filter
L_h	90 μH	Inductor of single tuned filter
C_h	22 μF	Capacitor of single tuned filter
R_h	0.09 Ω	Resistor of single tuned filter
R_p	1 MΩ	Resistor for detecting CMV
R_F	230 kΩ	Current-limiting resistor
R_C	4.7 kΩ	Pull-up resistor
L_{r1}	300 μH	Inductor of active filter
L_{r2}	30 μH	
C_{r1}	75 μF	Capacitor of active filter
C_{r2}	66 μF	
R_r	0.03 Ω	Resistor of active filter
f_0	50 Hz	Output power-frequency
f_c	3.6 kHz	Carrier frequency
$t_{\rm dead}$	5 μs	Switching dead-time of IGBT
$t_{\rm dead1}$	1 μs	Switching dead-time of P-MOSFET

V. EXPERIMENTS

In the experiments, the switches of the inverter's main circuit are implemented by insulated-gate bipolar transistors (IGBTs) and the switches of the active CM filter are implemented by P-MOSFETs. An induction motor, whose rated voltage is 380 V and rated power is 3 kW, is used as the load of the inverter. The other parameters of the experimental circuit (see Fig. 7) are listed in Table IV.

In the experiments, the detection-control scheme and the calculation-control scheme are implemented respectively in the processor as the control signals of the active filter's switches. In Fig. 5, the reference sinusoids $v_{\rm Aref}$, $v_{\rm Bref}$, $v_{\rm Cref}$, and the modulation index M_a come from the closed-loop control unit of the inverter. Some transmission gates are inserted into the signal paths in Fig. 5. Its purpose is to compensate for the XOR

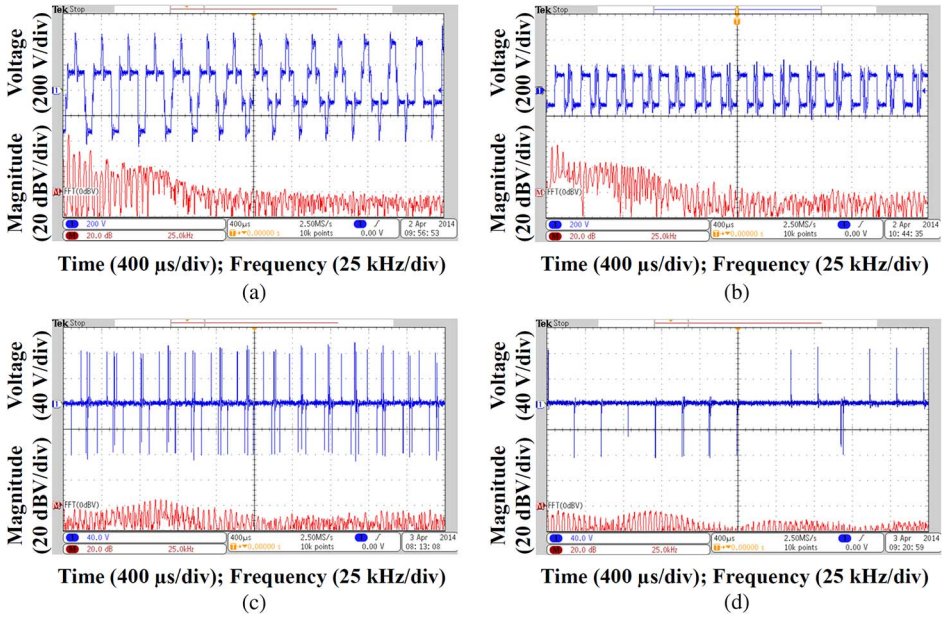

Fig. 8. Experimental results of the CMV $v_{\rm cm}$ (top) and its FFT (bottom) in the three-phase inverter without a hybrid filter (a) under the conventional SPWM strategy or (b) under the CPPM strategy, and (c) with the detection-control hybrid filter or (d) with the calculation-control hybrid filter under the CPPM strategy.

gate or NOT gate on the other paths and to balance the delay times on the different driving paths. The strategy of the inverter is implemented in a field-programmable gate array (FPGA).

In the three-phase inverter with CPPM, the detection-control scheme and calculation-control scheme are adopted to drive the hybrid filter respectively. To ensure that the experiments are carried out under the same load conditions, the detection-control module [as shown in Fig. 5(a)] is still retained in the main circuit when the active CM filter is driven by the calculation-control scheme block [as shown in Fig. 5(b)]. A manual switch is used to switch the driving signals ($S_{\rm rcm}$ and $\overline{S}_{\rm rcm}$) of the active CM filter between the output signals in Fig. 5(b) and the output signals of "Detection-control scheme" block in Fig. 5(a). The output CMV $v_{\rm cm}$, CMC $i_{\rm cm}$, and DMV $v_{\rm AB}$ are measured under the above two schemes. In order to observe the influence of the CMV on the motor shaft, the shaft voltages $v_{\rm shaft}$ of the motor are measured by a carbon brush. To compare with the above experimental results, $v_{\rm cm}$ and v_{AB} of the inverter without single tuned filter and active CM filter are also measured under the conventional SPWM strategy and the CPPM strategy, respectively.

Fig. 8 shows the output CMVs of the inverter under different conditions. Fig. 8(a) shows that the peaks of CMV (above 350 V and below -350 V) will appear in every carrier cycle under the conventional SPWM strategy. Under the CPPM strategy, the CMV wave is generally between -117 V and $+117$ V. Even if the overshoot of the jump edges is taken into consideration, the CMV peaks are not outside the range of ± 240 V [see Fig. 8(b)]. In order to analyze the CMV magnitudes at different frequencies, Fig. 8 also gives the calculated FFT by the oscilloscope. Under the conventional SPWM strategy, the maximal peak of the CMV in the frequency-domain is up to 44 dBV, whereas it is only about 36 dBV under the CPPM strategy.

Under the CPPM strategy, the output CMVs of the inverter with the hybrid filter are shown in Fig. 8(c) and (d). By using the detection-control or the calculation-control hybrid filter, in the CMV there are only some spikes, whose duration is of microsecond level. The spikes do not exceed ± 100 V. Due to the detection-control delay and the switching dead-time of the active filter, in the CMV there will appear a spike of 0.5–1.5 μs at every switching moment of the active filter's switches. As a result, the CMV spikes appear much more frequently in Fig. 8(c). Due to the switching dead-time of IGBTs and P-MOSFETs, in the CMV with calculation-control scheme, there will also be some spikes which are slightly wider than that with detection-control scheme. The experimental results [see Fig. 8(d)] show that the negative effects of the switching dead-time on CMV filtering do not occur at every switching moment and just appear one time per carrier cycle, which is much lower than the occurrence frequency of the spikes by using detection-control scheme. The FFT results in Fig. 8(c) and (d) show that the peak of the output CMV spectrum in the inverter with the hybrid filter is greatly lower than that without the hybrid filter [Fig. 8(b)]. The FFT results of the maximal peak also make it clear that the hybrid filter under the calculation-control scheme [about -4 dBV in Fig. 8(d)] is superior to that under the detection-control scheme [about $+5$ dBV in Fig. 8(c)].

The shaft voltages of the motor, which is driven by the three-phase inverter under different conditions, are shown in Fig. 9. As the shaft voltage is coupled from the CMV through the distributed capacitance between the stator and the rotor in the motor, the shaft voltage waveform and CMV waveform are very similar except for their different magnitudes. Similar to the CMV results, the harm of the shaft voltage in the three-phase inverter driven motor system with the hybrid filter is less than that without the hybrid filter. To drive the hybrid filter, the suppression effect of the shaft voltage through the calculation-control scheme is better than that through the detection-control scheme. Its maximal spikes are only about ± 4 V [as shown in Fig. 9(c)].

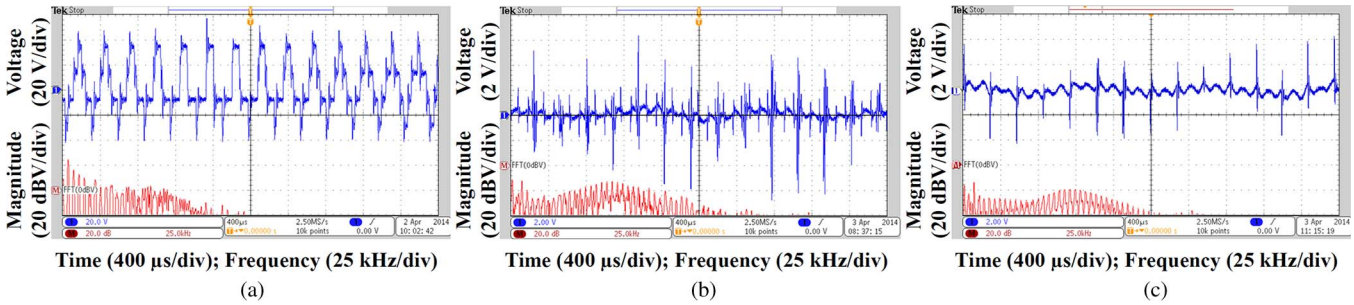

Fig. 9. Experimental results of the shaft voltage $v_{\rm shaft}$ (top) and its FFT (bottom) in the three-phase inverter (a) under the conventional SPWM strategy without a hybrid filter, and under the CPPM strategy (b) with the detection-control hybrid filter or (c) with the calculation-control hybrid filter.

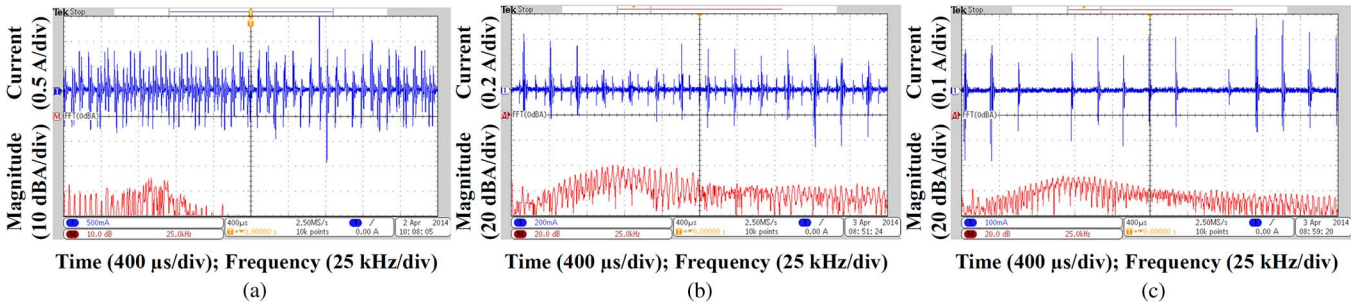

Fig. 10. Experimental results of the CMC $i_{\rm cm}$ (top) and its FFT (bottom) in the three-phase inverter (a) under the conventional SPWM strategy without a hybrid filter, and under the CPPM strategy (b) with the detection-control hybrid filter or (c) with the calculation-control hybrid filter.

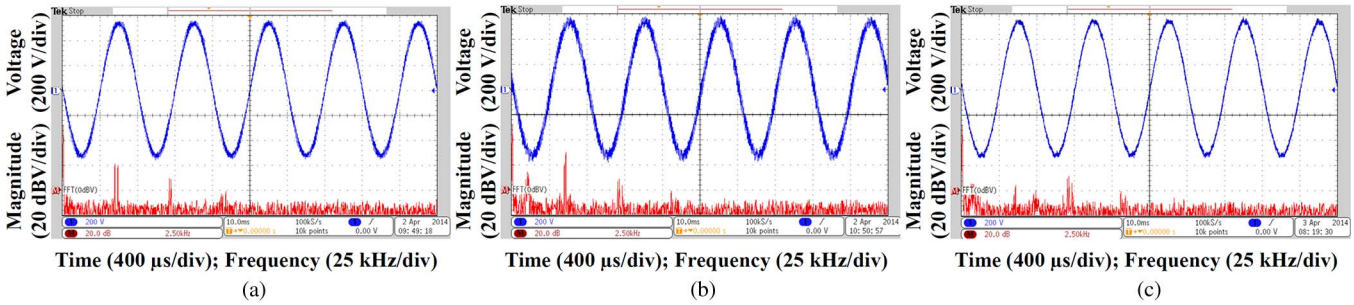

Fig. 11. Experimental results of the DMV v_{AB} (top) and its FFT (bottom) in the three-phase inverter (a) under the conventional SPWM strategy or (b) under the CPPM strategy without a hybrid filter, and (c) under the CPPM strategy with the hybrid filter.

Fig. 10 shows the output CMCs of the inverter under different conditions. The peaks of CMC are derived from dv/dt of the CMV jump edges. Under the conventional SPWM strategy, each jump step of the CMV is greater than 233 V and forms high CMC peak [$>$ 1.5 A, see Fig. 10(a)]. The experimental FFT result of its CMC shows that the maximal peak in the frequency domain is about -24 dBA. After the hybrid filter is added in the three-phase inverter, the CMC peaks are decreased obviously. Under the calculation-control scheme, the spikes of the CMC are less than ± 300 mA [see Fig. 10(c)]. In the frequency domain, the maximal peak of the CMC is reduced to -40 dBA under the detection-control scheme and to -44 dBA under the calculation-control scheme. This verifies that the hybrid filter can effectively suppress the output CMC and decrease the interference on the adjacent equipments so as to avoid malfunction.

Fig. 11 shows the output DMV v_{AB} in the inverter under different conditions. The FFT results in Fig. 11(a) and (b) confirm the previous simulation conclusion: the major harmonics of the DMV are near the carrier frequency. Under the conventional SPWM strategy and the CPPM strategy without a hybrid filter, the maximal magnitudes of the DM harmonics are 20 dBV and 30 dBV respectively. As shown in Fig. 11(c), the harmonic peak of the DMV in the carrier frequency band is reduced by more than 20 dBV while the hybrid filter is added. Table V lists the THD of the output DMV in the inverter under three conditions. After using the hybrid filter, the THD under the CPPM strategy is reduced from above 9% to below 2.5%, which can meet the demand of most loads for the output AC voltage of the inverter.

TABLE V
EXPERIMENTAL THD OF OUTPUT LINE–LINE VOLTAGE

Condition	Without a hybrid filter		With the hybrid filter
	Conventional SPWM strategy	CPPM strategy	CPPM strategy
THD	4.43%	9.15%	2.46%

In order to evaluate quantitatively the hybrid filter's effect on the improvement of the inverter's output in the frequency domain, the CMV and DMV are measured by a spectrum analyzer after 1000 times attenuation (viz. -60 dB). As shown in Fig. 12, the maximal peak of CMV in the spectrum with

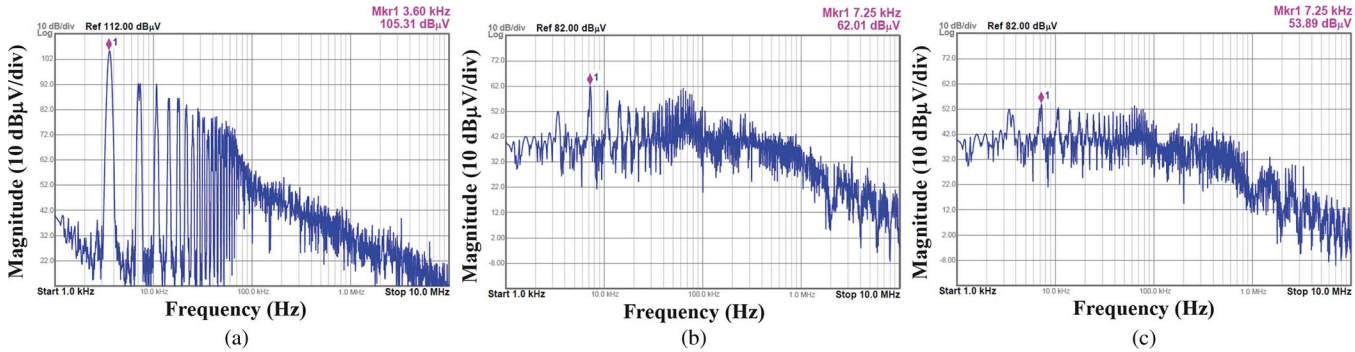

Fig. 12. Experimental spectra of the CMV $v_{\rm cm}$ in the three-phase inverter (a) under the conventional SPWM strategy without a hybrid filter, and under the CPPM strategy (b) with the detection-control hybrid filter or (c) with the calculation-control hybrid filter.

the hybrid filter under the CPPM strategy is at least 40 dBμV lower than that without a hybrid filter under the conventional SPWM strategy. On the whole, the peaks in Fig. 12(b) and (c) in the low frequency range (1 kHz–100 kHz) are 20 dBμV or more lower than those in Fig. 12(a). In the low frequency range, the spectral peaks of the CMV with the calculation-control hybrid filter are further suppressed by about 10 dBμV in comparison with the detection-control hybrid filter. Compared with the spectrum under the conventional SPWM strategy in the high frequency range (100 kHz–10 MHz), the spectrum with the detection-control hybrid filter under the CPPM strategy is not improved markedly, but the spectrum with the calculation-control hybrid filter under the CPPM strategy is improved by about 5–8 dBμV. Therefore, with the hybrid filter, the spectrum of the CMV is improved visibly in the low frequency range and is not improved much in the high frequency range. But the suppression effect of the CMV with the calculation-control hybrid filter under the CPPM strategy is outstanding no matter it is in the low frequency range or in the high frequency range.

Fig. 13 shows the spectra of the output DMV in the inverter with and without the hybrid filter. It can be seen that the major suppression of DMV locates near the carrier frequency. The improvement of the DMV in other frequency region is not conspicuous. Because the output THD of the inverter is the most important indicator, the suppression design of DMV focuses on the maximal peak in frequency domain (viz. near the carrier frequency). In this experiment, the DMV harmonics in other frequency region have little effect on the THD. Thus, the hybrid filter reduces the THD efficiently by suppressing the peaks near the carrier frequency.

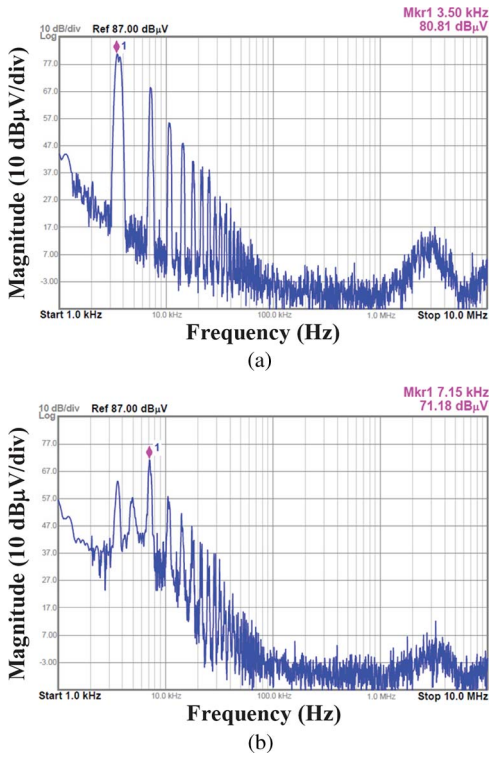

Fig. 13. Experimental spectra of the DMV v_{AB} in the three-phase inverter (a) under the conventional SPWM strategy without a hybrid filter, and (b) under the CPPM strategy with the hybrid filter.

VI. Conclusion

Through the above analysis and experiments, the hybrid filter, which is designed in this paper to suppress the CMV and DM harmonics of the three-phase inverter, is proved to have the following characteristics.

1) Simple in structure: Because it is ensured that the output CMV of the inverter can be two levels in any case by using the CPPM strategy, the simple half bridge is used in the hybrid filter to counteract the CMV. The simple structure means lower cost.
2) Easy in installation: As the added active DMV filter and single tuned filter in the hybrid filter are paralleled into the output lines of the inverter, they can be installed conveniently and are very suitable for the revamping of the established system.
3) Flexible in application: The proportional coefficient k provides the flexibility for the application design of the hybrid filter in various power levels.
4) Optimized in effect: As for the CMV suppression effect, the inverter with the hybrid filter is much better than that without the hybrid filter and the hybrid filter under the calculation-control scheme is superior to that under the detection-control scheme.
5) Compatible in THD standard: The phase-shifting of the carrier in the CPPM strategy enhances the output DM harmonics of the inverter in the carrier frequency band. Adding a single tuned filter in the hybrid filter suppresses the harmonics well and makes the output sinusoidal voltage meet the THD demand of loads.

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Jin Huang (M'14) was born in Wuhan, China, in 1970. He received the B.S. degree from Shanghai Jiaotong University, Shanghai, China, in 1992, and the M.S. and Ph.D. degrees from Huazhong University of Science and Technology, Wuhan, China, in 2003 and 2009, respectively.

He is currently an Associate Professor with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology. His research interests are control techniques, EMC, and reliability of power electronics devices.

Haixia Shi was born in Wuhan, China, in 1972. She received the Bachelor's degree from Wuhan University, Wuhan, China, in 1995, and the M.Tech. degree from Central China Normal University, Wuhan, in 2003.

Since 2003, she has been a Lecturer with Wuhan Textile University, Wuhan.